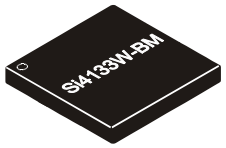
Si4133W

RF Synthesizer with Integrated VCOs for W-CDMA and GSM/UMTS Wireless Communications

Features

- Dual RF synthesizers
  - RF1: 2.3 GHz to 2.6 GHz
  - RF2: 750 MHz to 1.7 GHz
- IF synthesizer
  - IF: 62.5 MHz to 1.0 GHz
- Integrated VCOs, loop filters, dividers, and phase detectors
- Minimal external components
- Continuous operation over a wide temperature range
- Fast settling time: 200 μsec
- Low phase noise
- 5 μA standby current
- 28-lead MLP, 5 x 5 mm



Ordering Information:

See page 28.

Applications

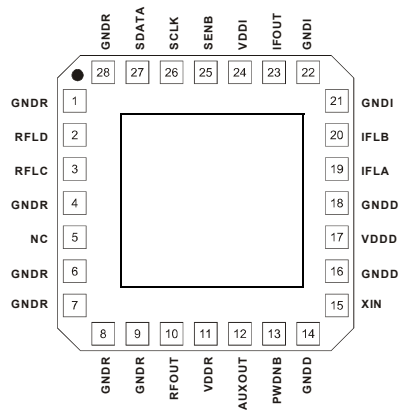
- Single-mode W-CDMA wireless handsets, terminals, and modems
- Dual-mode GSM/UMTS wireless handsets, terminals, and modems

Description

The Si4133W is a monolithic integrated circuit that performs RF and IF synthesis for GSM/GPRS and W-CDMA wireless communications. In dual-mode GSM/UMTS handsets, the Si4133W meets demanding requirements for very low phase noise and fast settling time for both modes. The Si4133W integrates three complete phase-locked loops (PLLs) on a single die including VCOs, loop filters, reference and VCO dividers, and phase detectors. Dividers and powerdown settings are programmable through a three-wire serial interface.

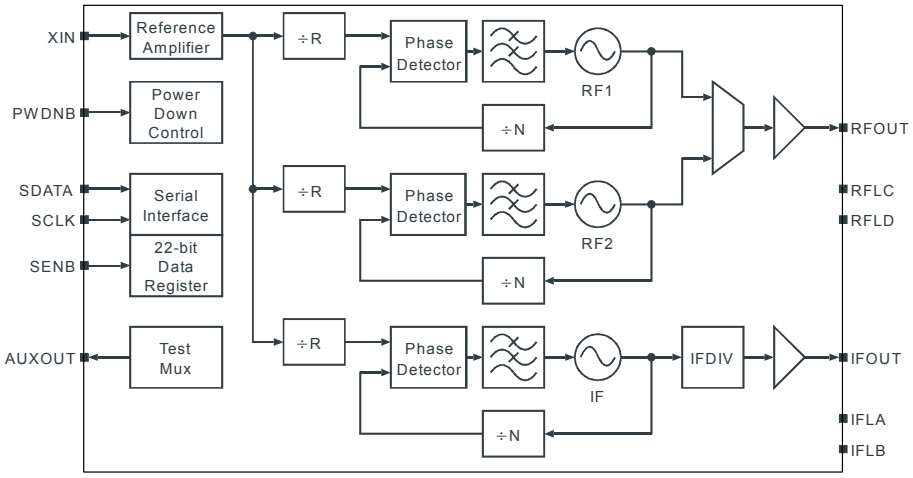
Pin Assignments

Si4133W-BM



Patents pending

Functional Block Diagram



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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–25	25	85	°C
Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Supply Voltages Difference	V_Δ	$(V_{DDR} – V_{DDD})$, $(V_{DDI} – V_{DDD})$	–0.3	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 4.0	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	–55 to 150	°C

Note:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **This device is a high performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDATA, SENB, PWDNB and XIN.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –25 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Typical Supply Current[1]		RF1 and IF operating	—	23	27.5	mA
RF1 Mode Supply Current[1]			—	15	18	mA
RF2 Mode Supply Current[1]			—	12	15	mA
IF Mode Supply Current[1]			—	9	11.5	mA
Standby Current		PWDNB = 0	—	5	—	µA
High Level Input Voltage[2]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[2]	I_{IH}	V_{IH} = 3.6 V, V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD}= 3.6 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OH} = 500 µA	—	—	0.4	V

Notes:
1. RF1 = 2.4 GHz, RF2 = 1.6 GHz, IFOUT = 800 MHz, LPWR = 0.
2. For signals SCLK, SDATA, SENB, and PWDNB.
3. For signal AUXOUT.

Table 4. Serial Interface Timing
(V_{DD} = 2.7 to 3.6 V, T_A = –25 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 1	40	—	—	ns
SCLK Rise Time	t_r	Figure 1	—	—	50	ns
SCLK Fall Time	t_f	Figure 1	—	—	50	ns
SCLK High Time	t_h	Figure 1	10	—	—	ns
SCLK Low Time	t_l	Figure 1	10	—	—	ns
SDATA Setup Time to SCLK↑[2]	t_{su}	Figure 2	5	—	—	ns
SDATA Hold Time from SCLK↑[2]	t_{hold}	Figure 2	0	—	—	ns
SENB↓ to SCLK↑ Delay Time[2]	t_{en1}	Figure 2	10	—	—	ns
SCLK↑ to SENB↑ Delay Time[2]	t_{en2}	Figure 2	12	—	—	ns
SENB↑ to SCLK↑ Delay Time[2]	t_{en3}	Figure 2	12	—	—	ns
SENB Pulse Width	t_w	Figure 2	10	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of the waveform. See Figure 2.

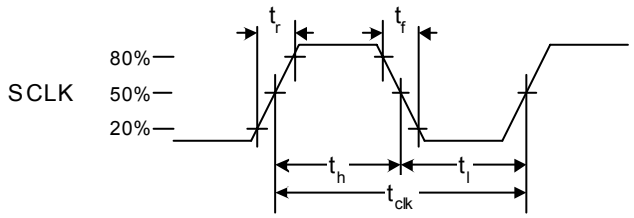


Figure 1. SCLK Timing Diagram

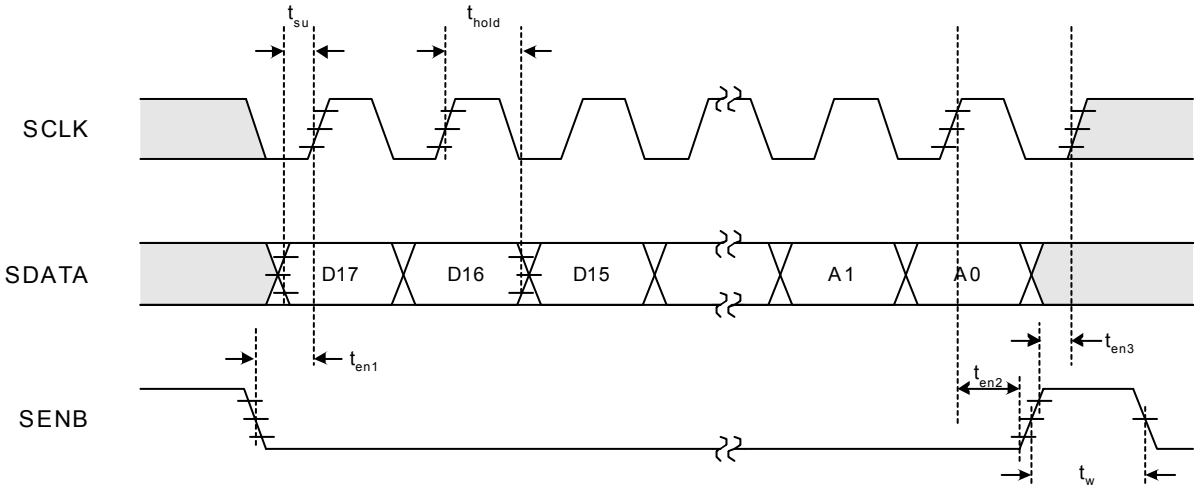


Figure 2. Serial Interface Timing Diagram

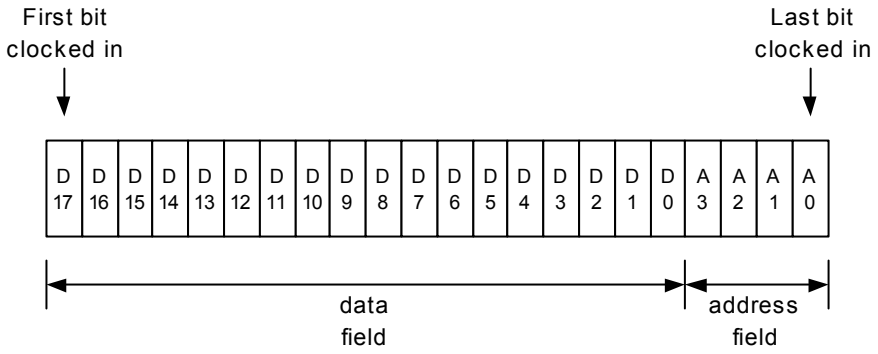


Figure 3. Serial Interface Format

Table 5. Si4133W RF and IF Synthesizer Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –25 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}		2	—	40	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	V_{DD} +0.3 V	V_{PP}
Phase Detector Update Frequency[2]	f_ϕ	$f_\phi = f_{REF}/R$	10	—	250	kHz
RF1 VCO Tuning Range[3]			2300	—	2600	MHz
RF2 VCO Center Frequency Range[4]	f_{CEN}		789	—	1619	MHz
RF2 Tuning Range from f_{CEN}[5]		Note: L_{EXT} ±10%	–5	—	5	%
IF VCO Center Frequency Range	f_{CEN}		526	—	952	MHz
IFOUT Tuning Range from f_{CEN}		with IFDIV	62.5	—	1000	MHz
IFOUT VCO Tuning Range from f_{CEN}		Note: L_{EXT} ±10%	–5	—	5	%
RF1 VCO Pushing		Open loop	—	300	—	kHz/V
RF2 VCO Pushing			—	150	—	kHz/V
IF VCO Pushing			—	50	—	kHz/V
RF1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	150	—	kHz p-p
RF2 VCO Pulling			—	50	—	kHz p-p
IF VCO Pulling			—	10	—	kHz p-p
RF1 Phase Noise		1 MHz offset	—	–130	—	dBc/Hz
		5 MHz offset	—	–145	—	dBc/Hz
		10 MHz offset	—	–150	—	dBc/Hz
RF1 Integrated Phase Error		100 Hz to 1 MHz	—	1.7	—	degrees rms
RF2 Phase Noise		1 MHz offset	—	–132	—	dBc/Hz
RF2 Integrated Phase Error		100 Hz to 1 MHz	—	1.2	—	degrees rms

Notes:
1. f_ϕ = 200 kHz, RF1 = 2.4 GHz, RF2 = 1.5 GHz, IFOUT = 800 MHz, LPWR = 0, for all parameters unless otherwise noted.
2. Low update frequencies have a maximum value of N for stable operation. See Table 8 on page 18.
3. RF1 tuning range is fixed by inductance of internally bonded wires.
4. RF2 VCO center frequency is fixed by inductance of printed circuit board trace or external inductor. To properly design and layout the external inductor, see “AN31: Inductor Design for the Si41xx Synthesizer Family”.
5. Tuning range of externally tuned VCO assumes tolerance of L_{EXT} to ±10%. See “Setting the VCO Center Frequencies” on page 16.
6. From power up request (PWDNB↑ or SENB↑ during a write of 1 to bits PDIB and PDRB in Register 2) to synthesizer ready (settled to within 0.1 ppm frequency error).
7. From power down request (PWDNB↓, or SENB↑ during a write of 0 to bits PDIB and PDRB in Register 2) to supply current equal to I_{PWDN}.

Table 5. Si4133W RF and IF Synthesizer Characteristics (Continued)
(V_{DD} = 2.7 to 3.6 V, T_A = –25 to 85 °C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
IF Phase Noise		100 kHz offset	—	–115	—	dBc/Hz
IF Integrated Phase Error		100 Hz to 1 MHz	—	0.7	—	degrees rms
RF1 Harmonic Suppression		Second Harmonic	—	–28	–20	dBc
RF2 Harmonic Suppression			—	–23	–20	dBc
IF Harmonic Suppression			—	–26	–20	dBc
RFOUT Output Power Level		Z_L = 50 Ω, RF1 active	–8	–3	0.5	dBm
		Z_L = 50 Ω, RF2 active	–5	–1	1	dBm
IFOUT Output Power Level		Z_L = 50 Ω	–7.5	–4	–1	dBm
IF Output Voltage Level		Z_L = 200 Ω	—	0.30	—	V_{RMS}
RF1 Output Reference Spurs		Offset = 200 kHz	—	–65	—	dBc
		Offset = 400 kHz	—	–70	—	dBc
		Offset = 600 kHz	—	–75	—	dBc
RF2 Output Reference Spurs		Offset = 200 kHz	—	–65	—	dBc
		Offset = 400 kHz	—	–70	—	dBc
		Offset = 600 kHz	—	–75	—	dBc
Power Up Request to Synthesizer Ready Time, RF1/RF2/IF[6]	t_{pup}	Figure 4, Figure 5	—	200	—	µs
Power Down Request to Synthesizer Off Time, RF1/RF2/IF[7]	t_{pdn}	Figure 4, Figure 5	—	—	100	ns

Notes:
1. f_ϕ = 200 kHz, RF1 = 2.4 GHz, RF2 = 1.5 GHz, IFOUT = 800 MHz, LPWR = 0, for all parameters unless otherwise noted.
2. Low update frequencies have a maximum value of N for stable operation. See Table 8 on page 18.
3. RF1 tuning range is fixed by inductance of internally bonded wires.
4. RF2 VCO center frequency is fixed by inductance of printed circuit board trace or external inductor. To properly design and layout the external inductor, see “AN31: Inductor Design for the Si41xx Synthesizer Family”.
5. Tuning range of externally tuned VCO assumes tolerance of L_{EXT} to ±10%. See “Setting the VCO Center Frequencies” on page 16.
6. From power up request (PWDNB↑ or SENB↑ during a write of 1 to bits PDIB and PDRB in Register 2) to synthesizer ready (settled to within 0.1 ppm frequency error).
7. From power down request (PWDNB↓, or SENB↑ during a write of 0 to bits PDIB and PDRB in Register 2) to supply current equal to I_{PWDN}.

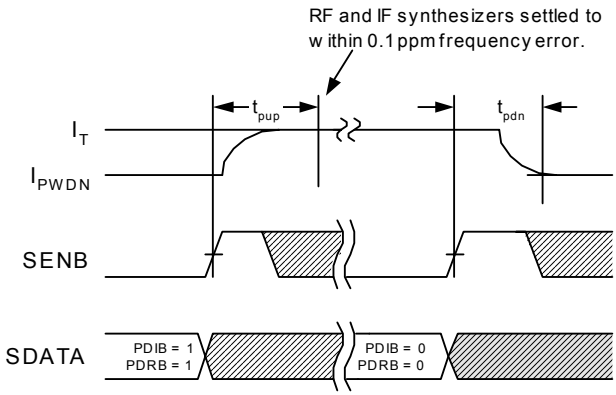


Figure 4. Software Power Management Timing Diagram

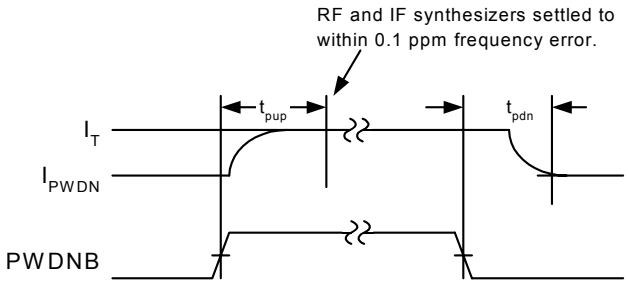


Figure 5. Hardware Power Management Timing Diagram

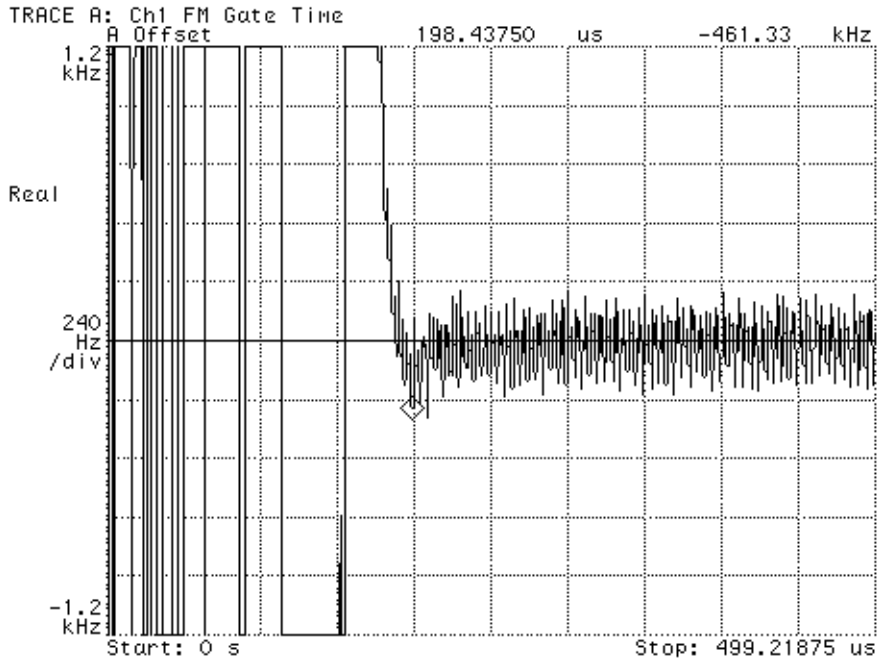


Figure 6. Typical Transient Response RF1 at 2.4 GHz with 200 kHz Phase Detector Update Frequency

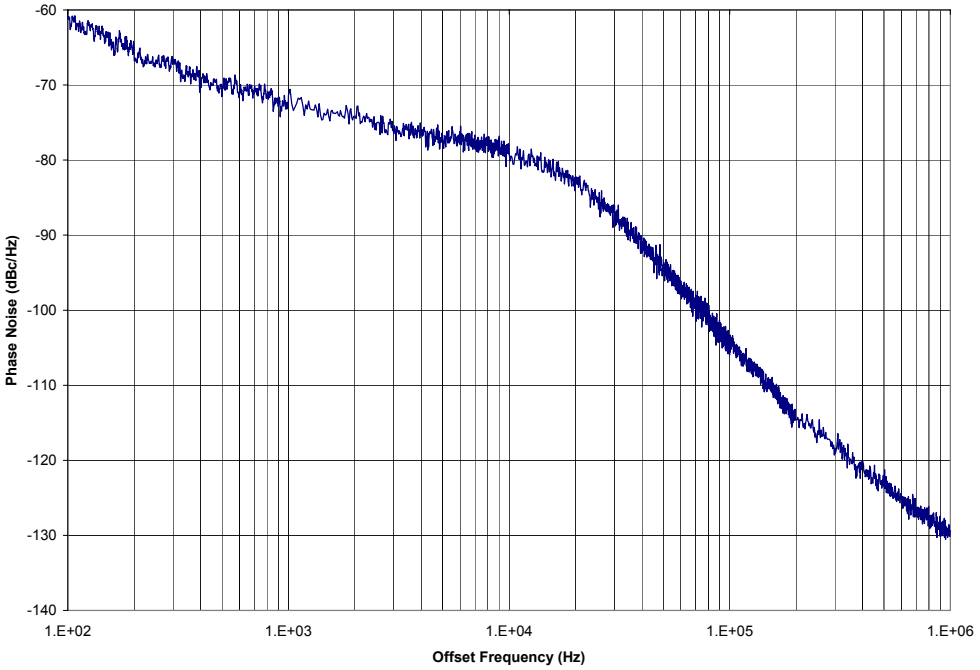


Figure 7. Typical RF1 Phase Noise at 2.4 GHz with 200 kHz Phase Detector Update Frequency

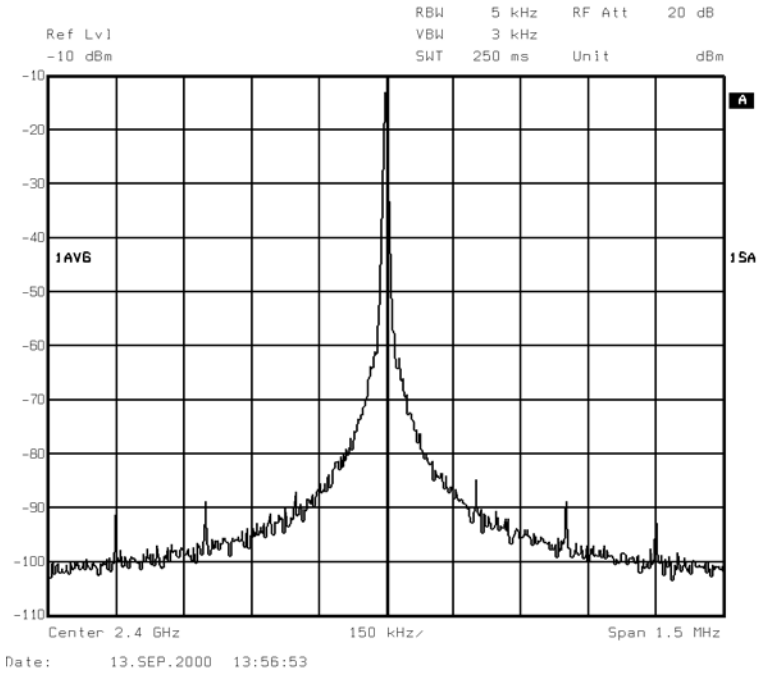


Figure 8. Typical RF1 Spurious Response at 2.4 GHz with 200 kHz Phase Detector Update Frequency

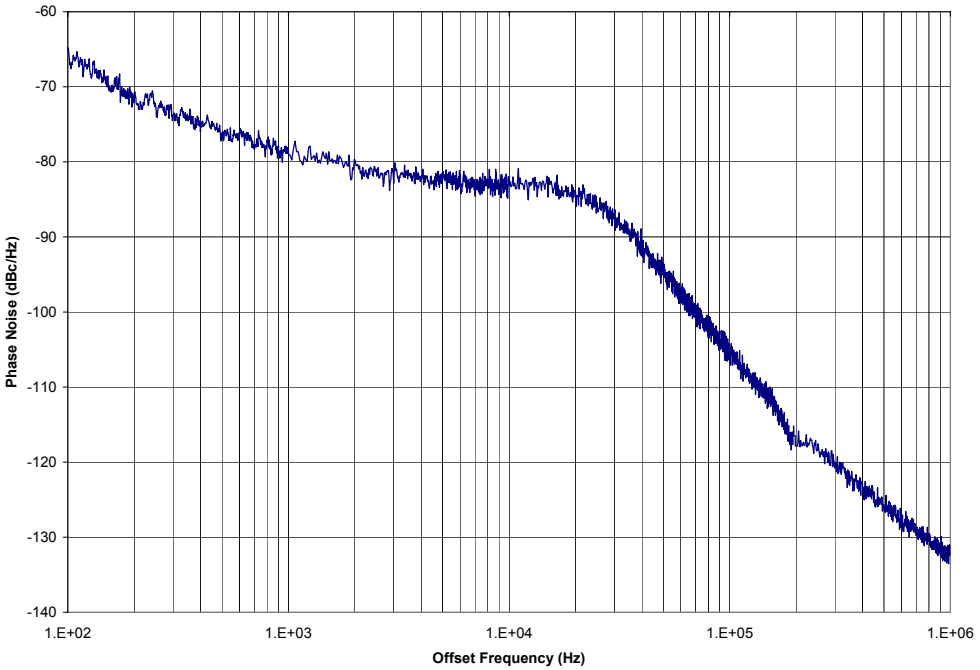


Figure 9. Typical RF2 Phase Noise at 1.6 GHz with 200 kHz Phase Detector Update Frequency

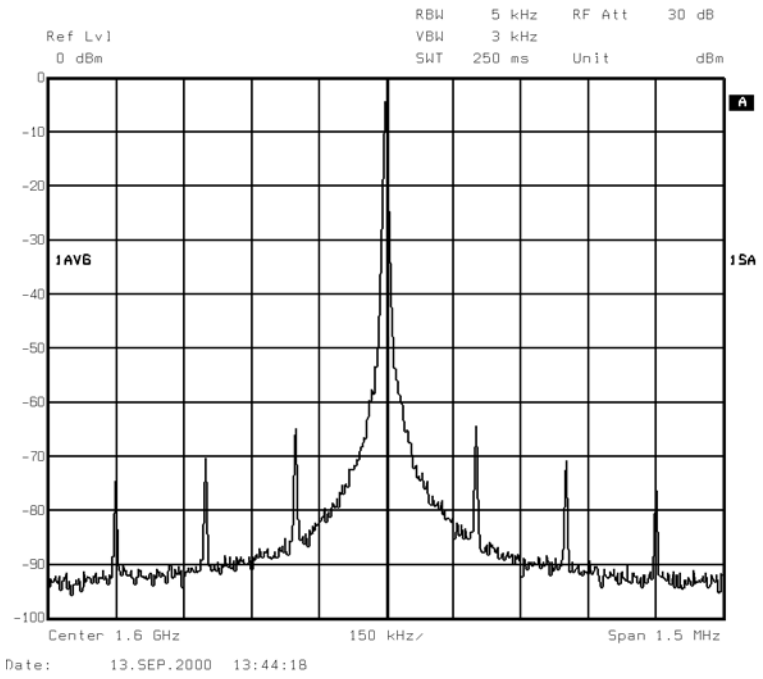


Figure 10. Typical RF2 Spurious Response at 1.6 GHz with 200 kHz Phase Detector Update Frequency

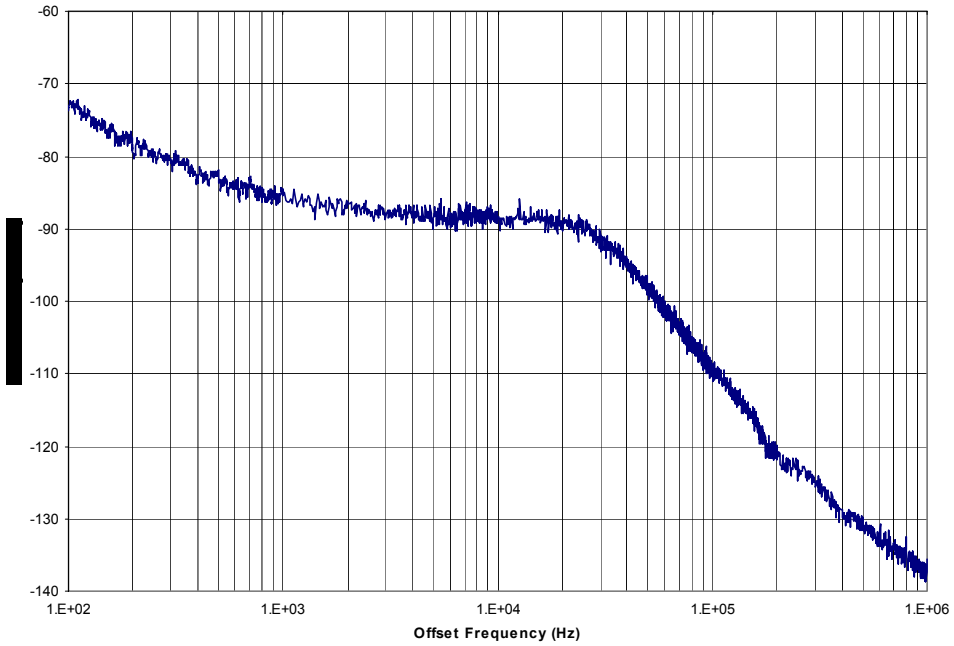


Figure 11. Typical IF Phase Noise at 800 MHz with 200 kHz Phase Detector Update Frequency

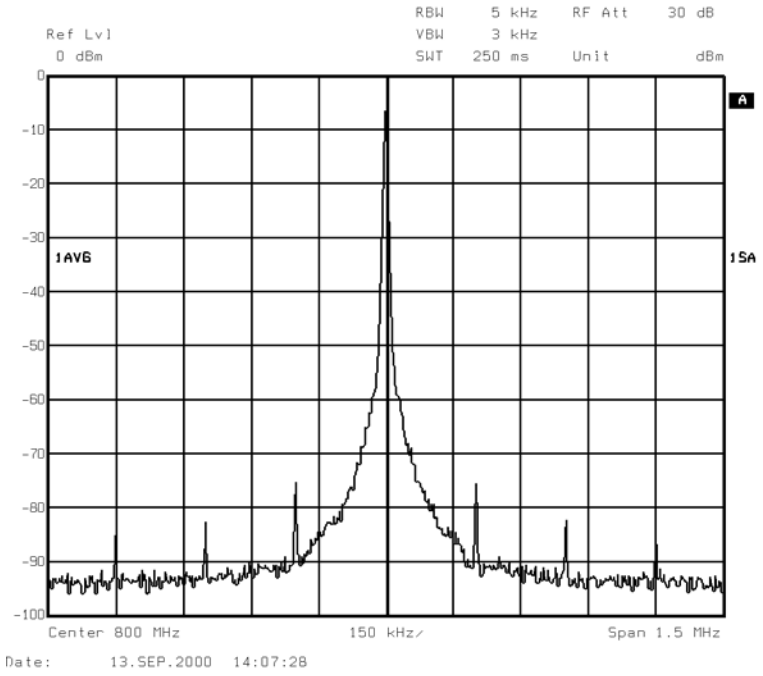
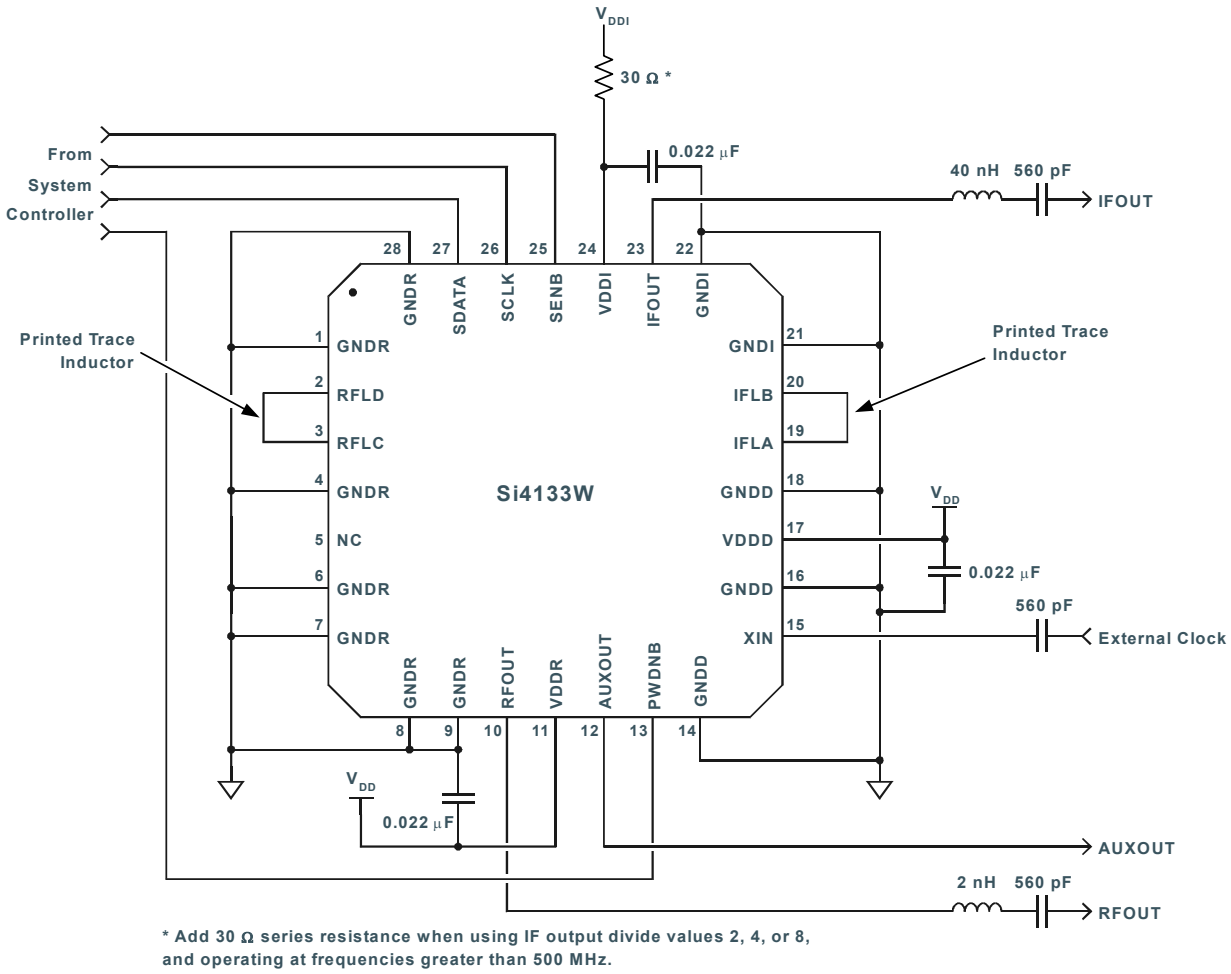


Figure 12. IF Spurious Response at 800 MHz with 200 kHz Phase Detector Update Frequency



* Add 30 Ω series resistance when using IF output divide values 2, 4, or 8, and operating at frequencies greater than 500 MHz.

Figure 13. Application Diagram

Functional Description

The Si4133W is a monolithic integrated circuit that performs IF and dual-band RF synthesis for W-CDMA communications applications. The Si4133W may be operated continuously over a wide ambient temperature range of –25 to +85 ^{O}C.

The Si4133W has three complete phase-locked loops (PLLs) with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4133W suitable for use in demanding wireless communications applications. Also integrated are phase detectors, loop filters, and reference and output frequency dividers. The IC is programmed through a three-wire serial interface.

Two PLLs are provided for dual-band RF synthesis. These RF PLLs are multiplexed so that only one PLL is active at a given time, as determined by the setting of an internal register. The active PLL is the last one written. The center frequency of the VCO in each PLL is set either by the internally bonded inductance within the package or by the value of an external inductance. For example, the Si4133W can have the RF2 center frequency set by an external inductor, while the RF1 center frequency is fixed by the inductance of internal bond wires. Inaccuracies in these inductances are compensated for by the self-tuning algorithm. The Si4133W executes the algorithm following powerup or following a change in the programmed output frequency.

The RF2 PLL, whose frequency is set through an external inductance, can adjust the output frequency by ±5% of its VCO's center frequency when active. Because the two VCOs can be set to have widely separated center frequencies, the RF output can be programmed to service two widely separated frequency bands by programming the corresponding N-Divider. The Si4133W has the RF1 VCO optimized to operate from 2.3 to 2.6 GHz, while the RF2 VCO is optimized to have its center frequency set between 750 MHz and 1.7 GHz.

One PLL is provided for IF synthesis. The center frequency of this circuit's VCO is set by connection of an external inductance. The PLL can adjust the IF output frequency by ±5% of the VCO center frequency. Inaccuracies in the value of the external inductance are compensated for by the Si4133W's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered-up (by either the PWDNB pin or by software) and/or each time a new output frequency is programmed.

The IF VCO can have its center frequency set as low as 526 MHz and as high as 952 MHz. An IF output divider is provided to divide down the IF output frequencies, if needed. The divider is programmable, capable of dividing by 1, 2, 4, or 8.

The unique PLL architecture used in the Si4133W produces settling (lock) times comparable in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

Serial Interface

A timing diagram for the serial interface is shown in Figure 2 on page 7. Figure 3 on page 7 shows the format of the serial interface.

The Si4133W is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when SENB is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of SENB into the internal data register addressed in the address field. The serial interface is disabled when SENB is high.

Table 11 on page 21 summarizes the data register functions and addresses. The internal shift register will ignore any leading bits before the 22 required bits.

Setting the VCO Center Frequencies

The PLLs can adjust the IF and RF2 output frequencies ±5% of the center frequencies of their VCOs. The RF1 PLL has a fixed operating range due to the inductance set by the internally bonded wires. Each center frequency for IF and RF2 PLLs is established by the value of the total inductance (internal and/or external) connected to the respective VCO. Manufacturing tolerances of ±10% for the external inductances are acceptable. The Si4133W will compensate for inaccuracies in each inductance by executing a self-tuning algorithm following PLL powerup or following a change in the programmed output frequency.

Because the total tank inductance is in the low nH range, the inductance of the package needs to be considered in determining the correct external inductance. The total inductance (L_{TOT}) presented to each VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). Each VCO has a nominal capacitance (C_{NOM}) in parallel with the total inductance, and the center frequency is as follows:

$$f_{CEN} = \frac{1}{2\pi\sqrt{L_{TOT} \cdot C_{NOM}}}$$

or

$$f_{CEN} = \frac{1}{2\pi\sqrt{(L_{PKG} + L_{EXT}) \cdot C_{NOM}}}$$

Table 6 summarizes the characteristics of each VCO.

Table 6. Si4133W-BM VCO Characteristics

VCO	Fcen Range (MHz)		Cnom (pF)	Lpkg (nH)	Lext Range (nH)	
	Min	Max			Min	Max
RF2	789	1619	5.1	1.6	0.29	6.4
IF	526	952	6.8	1.6	2.5	11.9

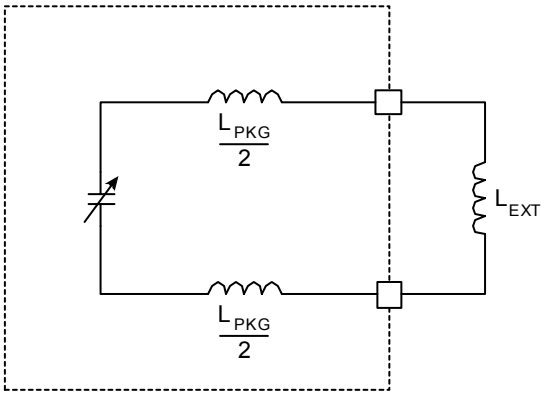


Figure 14. External Inductance Connection

As a design example, suppose synthesizing IFs in a 30 MHz band between 735 MHz and 765 MHz is desired. The center frequency should be defined as midway between the two extremes, or 750 MHz. The PLL will be able to adjust the VCO output frequency ±5% of the center frequency, or ±37.5 MHz of 750 MHz (i.e., from approximately 713 to 788 MHz). The IF VCO has a C_{NOM} of 6.8 pF. A 6.6 nH inductance (correct to two digits) in parallel with this capacitance will yield the desired center frequency. An external inductance of 5.0 nH should be connected between IFLA and IFLB, as shown in Figure 14. This, in addition to 1.6 nH of package inductance, will present the correct total inductance to the VCO. In manufacturing, the external inductance can vary ±10% of its nominal value and the Si4133W will correct for the variation with the self-tuning algorithm.

For more information on designing the external trace inductors, please refer to Application Note 31.

Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following power-up of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the desired output frequency. In doing so, the algorithm will compensate for manufacturing tolerance errors in the value of the external inductance connected to the VCO. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the PLL controls the VCO oscillation frequency. The PLL will complete frequency locking, eliminating any remaining frequency error. Thereafter, it will maintain frequency-lock, compensating for effects caused by temperature and supply voltage variations.

The Si4133W's self-tuning algorithm will compensate for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur *after* self-tuning is limited. For external inductances with temperature coefficients around ±150 ppm/^{o}C, the PLL will be able to maintain lock for changes in temperature of –50 to +80 ^{o}C from the temperature at which it initialized lock.

If the PLL is regularly powered down or the frequency is periodically reprogrammed, then this temperature range is of no concern because the VCO lock will be reinitiated. Lock-detect bar (LDETB) may be monitored on the AUXOUT pin for an indication that the PLL is about to run out of locking capability. (See "Auxiliary Output (AUXOUT)" for how to select LDETB.) The LDETB signal will be low after self-tuning has completed but will rise when either the IF or RF PLL nears the limit of its compensation range. LDETB will also be high when either PLL is executing the self-tuning algorithm. The output frequency will still be locked when LDETB goes high, but the PLL will eventually lose lock if the temperature continues to change in the same direction. Therefore, if LDETB goes high, both the IF and RF PLLs should promptly be re-tuned by initiating the self-tuning algorithm.

Output Frequencies

The IF and RF output frequencies are set by programming the R- and N-Divider registers. Each PLL has its own R and N registers so that each can be programmed independently. Programming either the R- or N-Divider register for RF1 or RF2 automatically selects the associated output.

The reference frequency on the XIN pin is divided by R and this signal is the input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by N. The PLL works to make these frequencies equal. That is, after an initial transient

$$\frac{f_{OUT}}{N} = \frac{f_{REF}}{R}$$

or

$$f_{OUT} = \frac{N}{R} \cdot f_{REF}$$

The integers R are set by programming the RF1 R-Divider register (Register 6), the RF2 R-Divider register (Register 7) and the IF R-Divider register (Register 8). The values of R are limited to the range of about 7 (decimal) to 8189 depending on the phase detector gain (see Registers 6–8 on pages 25 and 26.)

The integers N are set by programming the RF1 N-Divider register (Register 3), the RF2 N-Divider register (Register 4), and the IF N-Divider register (Register 5).

Each N-Divider is implemented as a conventional high speed divider. That is, it consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter.

PLL Loop Dynamics

The transient response for each PLL is determined by its phase detector update rate f_ϕ (equal to f_{REF}/R) and the phase detector gain programmed for each RF1, RF2, or IF synthesizer. (See Register 1.) Four different settings for the phase detector gain are available for each PLL. The highest gain is programmed by setting the two phase detector gain bits to 00 and the lowest by setting the bits to 11. The values of the available gains relative to the highest gain are shown in Table 7.

Table 7. Gain Values (Register 1)

K_P Bits	Relative P.D. Gain
00	1
01	1/2
10	1/4
11	1/8

The gain value bits must be set manually by writing to Register 1. In general, a higher phase detector gain will increase the speed of the PLL transient until the point at which stability begins to be compromised. The optimal gain depends on N. Table 8 lists recommended settings for different values of N. For large values of N, the output may become unstable as indicated by "x". In that case, to avoid unstable operation, it is recommended to increase the phase detector update rate (by lowering R or increasing f_{REF}) to achieve the same output frequency.

Table 8. Optimal K_P Settings

N	RF1 K_{P1}<1:0>	RF2 K_{P2}<3:2>	IF K_{PI}<5:4>
≤1023	00	00	00
1024–2047	00	00	01
2048–4095	00	01	10
4096–8191	01	10	11
8192–16383	10	11	11
16384–24575	11	11	11
24576–57343	11	11	x
57344–98303	11	x	x
≥98304	x	x	x
Note: The "x" indicates possible unstable operation.			

The VCO gain and loop filter characteristics are not programmable.

The settling time for the PLL is directly proportional to its phase detector update period T_ϕ ($T_\phi = 1/f_\phi$). During the first 13 update periods the Si4133W executes the self-tuning algorithm. Thereafter the PLL controls the output frequency. Because of the unique architecture of the Si4133W PLLs, the time required to settle the output frequency to 0.1 ppm error is only about 25 update periods. Thus, the total time after power-up or a change in programmed frequency until the synthesized frequency is well settled—including time for self-tuning—is around 40 update periods.

RF and IF Outputs (RFOUT and IFOUT)

The RFOUT and IFOUT pins are driven by amplifiers that buffer the RF VCOs and IF VCO, respectively. The RF output amplifier receives its input from either the RF1 or RF2 VCO, depending upon which R- or N-Divider register was last written. For example, programming the N-Divider register for RF1 automatically selects the RF1 VCO output.

Figure 13 on page 15 shows an application diagram for the Si4133W. The RF output signal must be coupled to its load through an ac coupling capacitor. An external inductance between the RFOUT pin and the ac coupling capacitor is required as part of an output matching network to maximize power delivered to the load. This 2 nH inductance may be realized with a PC board trace. The network is made to provide an adequate match to an external 50 Ω load for both the RF1 and RF2 frequency bands. The matching network also filters the output signal to reduce harmonic distortion.

The IFOUT pin must also be coupled to its load through an ac coupling capacitor. The IF output level is dependent upon the load. Figure 17 displays the output level versus load resistance for a variety of output frequencies. For resistive loads greater than 500 Ω the output level saturates and the bias currents in the IF output amplifier are higher than they need to be. The LPWR bit in the Main Configuration register (Register 0) can be set to 1 to reduce the bias currents and therefore reduce the power dissipated by the IF amplifier. For loads less than 500 Ω, LPWR should be set to 0 to maximize the output level.

For IF frequencies greater than 500 MHz, a matching network is required in order to drive a 50 Ω load. See Figure 15.

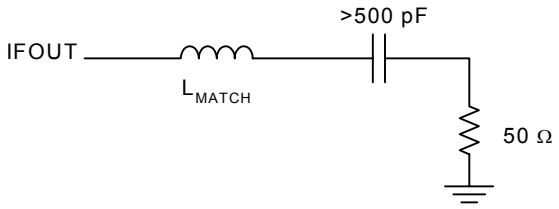


Figure 15. IF Frequencies > 500 MHz

Table 9. L_{MATCH} Values

Frequency	L_{MATCH}
500–600 MHz	40 nH
600–800 MHz	27 nH
800–1 GHz	18 nH

For frequencies less than 500 MHz, the IF output buffer can directly drive a 200 Ω resistive load or higher. For resistive loads greater than 500 Ω (f < 500 MHz) the LPWR bit can be set to reduce the power consumed by the IF output buffer. See Figure 16.

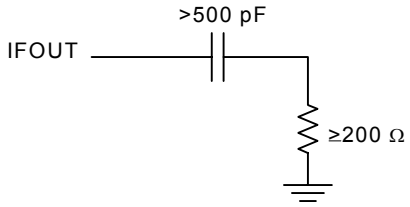


Figure 16. IF Frequencies < 500 MHz

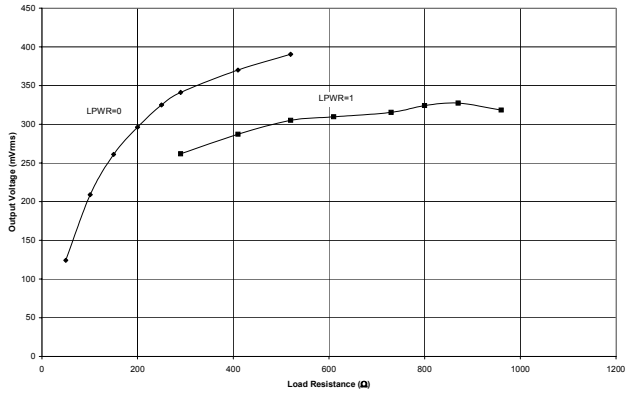


Figure 17. IF Output Voltage vs. Load

Reference Frequency Amplifier

The Si4133W provides a reference frequency amplifier. If the driving signal has CMOS levels, it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be ac coupled to the XIN pin through a 560 pF capacitor.

Power Down Modes

Table 10 summarizes the power down functionality. The Si4133W can be powered down by taking the PWDNB pin low or by setting bits in the Powerdown register (Register 2). When the PWDNB pin is low, the Si4133W

will be powered down regardless of the Powerdown register settings. When the PWDNB pin is high, power management is under control of the Powerdown register bits.

The reference frequency amplifier, IF, and RF sections of the Si4133W circuitry can be individually powered down by setting the Power Down register bits PDIB and PDRB low. Also, setting the AUTOPDB bit to 1 in the Main Configuration register (Register 0) is equivalent to setting both bits in the Powerdown register to 1. The serial interface remains available and can be written in all power down modes.

When multiple Si4133Ws are driven by a single reference oscillator, as in variable duplex W-CDMA applications, additional bits may be set in the control registers to prevent unwanted interaction during power down. For further information please refer to Application Note 44.

Auxiliary Output (AUXOUT)

The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration register (Register 0).

The LDETB signal can be selected by setting the AUXSEL bits to 11b. This signal can be used to indicate that the IF or RF PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned.

Table 10. Power Down Configuration

PWDNB Pin	AUTOPDB	PDIB	PDRB	IF Circuitry	RF Circuitry
PWDNB = 0	X	X	X	OFF	OFF
PWDNB = 1	0	0	0	OFF	OFF
	0	0	1	OFF	ON
	0	1	0	ON	OFF
	0	1	1	ON	ON
	1	x	x	ON	ON

Control Registers

Table 11. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	0	0	0	0	AUXSEL[1:0]		IFDIV[1:0]		0	0	0	0	LPWR	0	AUTO PDB	0	1	0
1	Phase Detector Gain	0	0	0	0	0	0	0	0	0	0	0	0	K_{PI}[1:0]		K_{P2}[1:0]		K_{P1}[1:0]	
2	Powerdown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB
3	RF1 N-Divider	N_{RF1}[17:0]																	
4	RF2 N-Divider	0	N_{RF2}[16:0]																
5	IF N-Divider	0	0	N_{IF}[15:0]															
6	RF1 R-Divider	0	0	0	0	0	R_{RF1}[12:0]												
7	RF2 R-Divider	0	0	0	0	0	R_{RF2}[12:0]												
8	IF R-Divider	0	0	0	0	0	R_{IF}[12:0]												
9	Reserved																		
. . .																			
15	Reserved																		

Note: Registers 9–15 are reserved. Writes to these registers may result in unpredictable behavior.

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0		AUXSEL[1:0]		IFDIV[1:0]		0	0	0	0	LPWR	0	AUTO PDB	0	1	0

Bit	Name	Function
17:14	Reserved	Program to zero.
13:12	AUXSEL[1:0]	**Auxiliary Output Pin Definition.** 00 = Reserved. 01 = Force output low. 10 = Reserved. 11 = Lock Detect (LDETB).
11:10	IFDIV[1:0]	**IF Output Divider.** 00 = IFOUT = IFVCO Frequency 01 = IFOUT = IFVCO Frequency/2 10 = IFOUT = IFVCO Frequency/4 11 = IFOUT = IFVCO Frequency/8
9:6	Reserved	Program to zero.
5	LPWR	**Output Power-Level Settings for IF Synthesizer Circuit.** 0 = $R_{LOAD} < 500\ \Omega$—normal power mode. 1 = $R_{LOAD} \geq 500\ \Omega$—low power mode.
4	Reserved	Program to zero.
3	AUTOPDB	**Auto Power Down.** 0 = Software powerdown is controlled by Register 2. 1 = Equivalent to setting all bits in Register 2 = 1.
2	Reserved	Program to zero.
1	Reserved	Program to one.
0	Reserved	Program to zero.

Register 1. Phase Detector Gain Address Field (A[3:0]) = 0001

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	K_{PI}[1:0]		K_{P2}[1:0]		K_{P1}[1:0]	

Bit	Name	Function
17:6	Reserved	Program to zero.
5:4	K_{PI}[1:0]	**IF Phase Detector Gain Constant.** N Value K_{PI} <1024 = 00 1024–2047 = 01 2048–4095 = 10 >4095 = 11
3:2	K_{P2}[1:0]	**RF2 Phase Detector Gain Constant.** N Value K_{P2} <2048 = 00 2048–4095 = 01 4096–8191 = 10 >8191 = 11
1:0	K_{P1}[1:0]	**RF1 Phase Detector Gain Constant.** N Value K_{P1} <4096 = 00 4096–8191 = 01 8192–16383 = 10 >16383 = 11

Register 2. Powerdown Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB

Bit	Name	Function
17:2	Reserved	Program to zero.
1	PDIB	**Power Down IF Synthesizer.** 0 = IF synthesizer powered down. 1 = IF synthesizer on.
0	PDRB	**Power Down RF Synthesizer.** 0 = RF synthesizer powered down. 1 = RF synthesizer on.
Note: Enabling any PLL with PDIB or PDRB will automatically power on the reference amplifier.		

Register 3. RF1 N-Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_{RF1}[17:0]																	

Bit	Name	Function
17:0	N_{RF1}[17:0]	**N-Divider for RF1 Synthesizer.**

Register 4. RF2 N-Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	N_{RF2}[16:0]																

Bit	Name	Function
17	Reserved	Program to zero.
16:0	N_{RF2}[16:0]	**N-Divider for RF2 Synthesizer.**

Register 5. IF N-Divider Address Field (A[3:0]) = 0101

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	N_{IF}[15:0]															

Bit	Name	Function
17:16	Reserved	Program to zero.
15:0	N_{IF}[15:0]	**N-Divider for IF Synthesizer.**

Register 6. RF1 R-Divider Address Field (A[3:0]) = 0110

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	R_{RF1}[12:0]												

	Name	Function
17:13	Reserved	Program to zero.
12:0	R_{RF1}[12:0]	**R-Divider for RF1 Synthesizer.** R_{RF1} can be any value from 7 to 8189 if K_{P1} = 00 8 to 8189 if K_{P1} = 01 10 to 8189 if K_{P1} = 10 14 to 8189 if K_{P1} = 11

Register 7. RF2 R-Divider Address Field (A[3:0]) = 0111

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	R_{RF2}[12:0]												

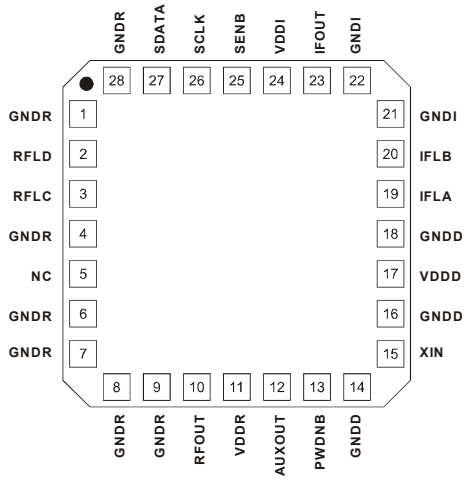
Bit	Name	Function
17:13	Reserved	Program to zero.
12:0	R_{RF2}[12:0]	**R-Divider for RF2 Synthesizer.** R_{RF2} can be any value from 7 to 8189 if K_{P2} = 00 8 to 8189 if K_{P2} = 01 10 to 8189 if K_{P2} = 10 14 to 8189 if K_{P2} = 11

Register 8. IF R-Divider Address Field (A[3:0]) = 1000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	R_{IF}[12:0]												

Bit	Name	Function
17:13	Reserved	Program to zero.
12:0	R_{IF}[12:0]	**R-Divider for IF Synthesizer.** R_{IF} can be any value from 7 to 8189 if K_{P1} = 00 8 to 8189 if K_{P1} = 01 10 to 8189 if K_{P1} = 10 14 to 8189 if K_{P1} = 11

Pin Descriptions: Si4133W-BM



Pin Number(s)	Name	Description
1,4, 6–9, 28	GNDR	Common ground for RF analog circuitry
2, 3	RFLC, RFLD	Pins for inductor connection to RF2 VCO
5	NC	No connect
10	RFOUT	Radio frequency (RF) output of the selected RF VCO
11	VDDR	Supply voltage for the RF analog circuitry
12	AUXOUT	Auxiliary output
13	PDWNB	Power down input pin
14, 16, 18	GNDD	Common ground for digital circuitry
15	XIN	Reference frequency amplifier input
17	VDDD	Supply voltage for digital circuitry
19–20	IFLA, IFLB	Pins for inductor connection to IF VCO
21–22	GNDI	Common ground for IF analog circuitry
23	IFOUT	Intermediate frequency (IF) output of the IF VCO
24	VDDI	Supply voltage for IF analog circuitry
25	SENB	Enable serial port input
26	SCLK	Serial clock input
27	SDATA	Serial data input

Ordering Guide

Ordering Part Number	Description	Operating Temperature
Si4133W-BM	2.4 GHz/RF2/IFOUT	–25 to 85 °C

Package Outline: Si4133W-BM

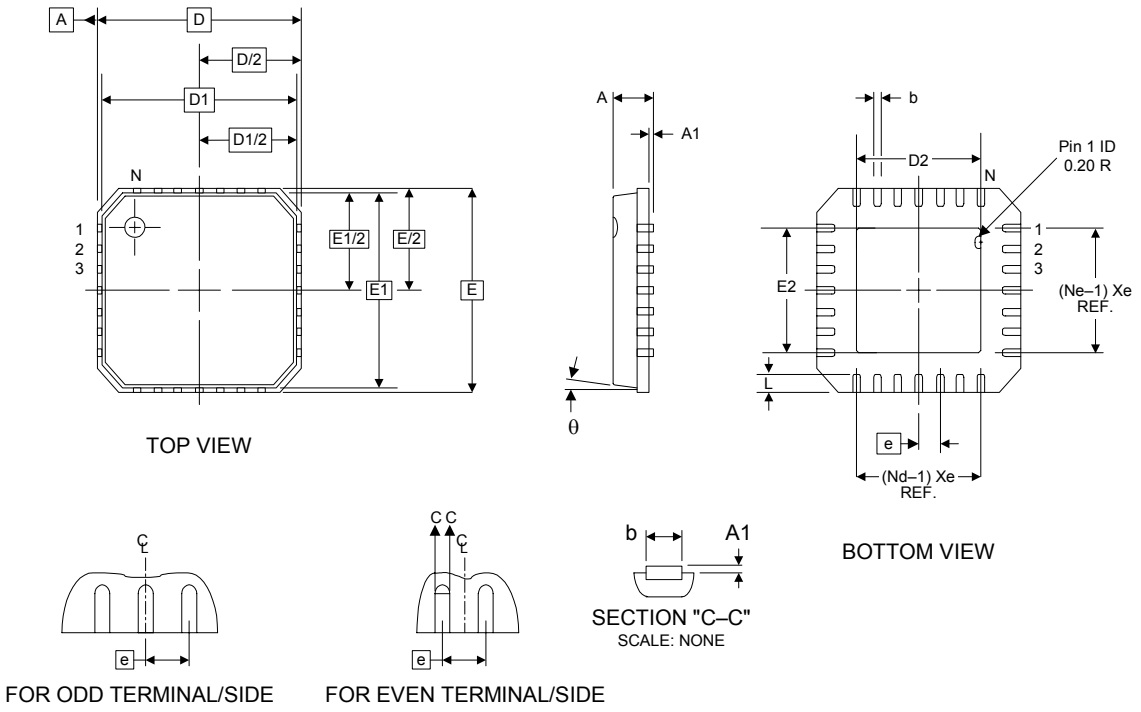


Figure 18. 28-Pin Micro Leadframe Package (MLP)

Table 12. Package Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	—	0.85	0.90
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D, E	5.00 BSC		
D1, E1	4.75 BSC		
D2, E2	2.55	2.70	2.85
N	28		
Nd	7		
Ne	7		
e	0.50 BSC		
L	0.50	0.60	0.75
θ			12°

Document Change List

Revision 1.0 to Revision 1.1

- Table 5 on page 8
  - RFOUT and IFOUT Output Power Level specifications have been updated
  - Note 1 RF2 spec changed to 1.5 GHz

Notes:

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